

Remarks

The Examiner objected to the term: "for storing a single grain for each channel" of claim 1 under 35 U.S.C. 112, on the basis that this term is vague and contradicts with the rest of the limitations in claim 1. Applicants have removed this term from claim 1, and the objection thereto is now believed to be moot.

Claims 1, 3 to 4, 7, 8, 10 –16, and 18-20 have been rejected under 35 USC 102 (e) as being anticipated by United States Patent No.7,113,505 (Williams) hereinafter referred to as Williams.

In response, Applicants have amended claim 1. A clean version of claim 1 is provided below for the Examiner's convenience:

1. A time division multiplexing switch comprising:
 - a plurality of ingress ports, each of the ingress ports in the plurality for synchronously receiving data grains at fixed time intervals, the data grains ordered as grain groups;
 - a plurality of memory egress self selection (MESS) egress ports, for receiving the data grains from the plurality of ingress ports, and transmitting the data grains in a predetermined order; and
 - a grain aggregator, operatively connected to the plurality of ingress ports, for aggregating the data grains received by each of the ingress ports during a single timeslot into an aggregate of data grains in an N grain wide channel, where N is the number of ingress ports, and for providing the aggregate of data grains to the plurality of MESS egress ports simultaneously;
 - each MESS egress port from the plurality having a data grain selector for selecting from the aggregate of data grains only data grains that the MESS egress port will transmit, prior to storing the selected grains for transmission by the MESS egress port;
 - said data grain selector being able to select up to N data grains during a single timeslot in accordance with at least one predetermined criterion being based on the ingress port associated with the received data grains and a position of a grain in its respective grain group.

The subject matter of amended claim 1 is fully supported by the application as originally filed at paragraphs [0028], [0029], [0039], and [0040], and Figures 7 - 9. Amended claim 1 now includes the subject matter of previous claim 3 which recites the use of an aggregator, and specifies the N grain wide channel in which aggregated data grains are simultaneously provided to the plurality of MESS egress ports. New claim 21 has features similar to other pending apparatus claims.

As recited in claim 1, the invention provides a time division multiplexing switch comprising a plurality of ingress ports, a plurality of memory egress self selection (MESS) egress ports, and a grain aggregator. Each ingress port synchronously receives data grains ordered as grain groups at fixed time intervals. The egress ports receive data grains from the plurality of ingress ports, and transmit them in a predetermined order. The grain aggregator is connected to the ingress ports, to aggregate the data grains received by each channel in a single timeslot into an aggregate of data grains in an N grain wide channel, where N is the number of ingress ports, and provides the aggregate to the plurality of MESS egress ports simultaneously.

Each MESS egress port includes a data grain selector that selects from the aggregate of data grains only the data grains that are of interest i.e. the data grains that it will transmit, and stores them for subsequent transmission. Since the aggregate includes all the data grains received at a given timeslot, and since the aggregate is provided to all the MESS egress ports, each MESS egress port can select up to N grains at each timeslot using the data grain selector. The operation of selecting data grains is performed in accordance with at least one predetermined criterion being based on the ingress port associated with the received data grains and the position of the grain in its respective grain group.

Williams describes mesh architecture for synchronous cross-connects using conventional time- space-time (TST) switches (TST switches disclosed in 1952, see col.6, lines 1-12) and time-slot-interchangers(TSI). The thrust of Williams is the configuration and control of the switches in a mesh architecture so as to avoid collision at the links (col.6, lines 35-45 & Fig.6). According to Williams, every sample of data received at a node is stored by the receiving node if the receiving node matches the intended destination of the sample. Otherwise, the sample is forwarded to the next node in the next timeslot (see cols.16-17 & Fig.15).

The invention recited in amended claim 1 is entirely different as will be described below:

Amended claim 1 recites a plurality of ingress ports for receiving data grains synchronously at fixed time intervals, and a grain aggregator that aggregates the grains received at the ingress ports in a single timeslot into an aggregate of data grains in an N grain wide channel, where N is the number of ingress ports. The Examiner considers that the time division multiplexing switch of Williams corresponds to the grain aggregator of the invention. Applicants respectfully disagree. The aggregator as recited in the claims aggregates the data grains received at the ingress ports during a single timeslot into an aggregate of data grains in an N grain wide channel, where N is the number of ingress ports. If each data grain received at each ingress port is one byte and the number of ingress ports is N, then the aggregate of data grains is an N byte word (see paragraph [0028], lines 1-9). By contrast, the time division multiplexing switch of Williams does not aggregate the data inputted thereto. Instead, like any other multiplexer, it outputs one sample of data at each timeslot not all the data samples provided at its input. Furthermore, the channel of Williams is not a wide channel that is able to transmit an aggregate of all the grains received at the input channels as recited in claim 1.

Additionally, amended claim 1 recites the feature of providing the aggregate of data grains to the plurality of MESS egress ports simultaneously. Figures 7 and 8 show that the ingress processors 206 of ingress ports 204 receive the data the data in parallel. Williams describes providing one sample of data to the node in one timeslot (see col.17 lines 13-18), which as disclosed in col.17 lines 45 - 48 requires long processing time when the number of channels is large.

Moreover, amended claim 1 recites that the data grain selector of each MESS egress port can select up to N data grains in a single timeslot where N is the number of ingress ports. Paragraph [0040] line 3 discloses that between 0 and N grains can be selected in any timeslot. By contrast, the nodes of Williams receive a single sample at each timeslot, and forward the sample to the next node in the next timeslot if the receiving node is not the destination node. Therefore, Williams does not disclose the feature of selecting a number of grains that equals the number of ingress ports in a single timeslot, as recited in claim 1.

Claim 1 also recites that each egress port includes a data grain selector which selects from the N grains (where N is the number of ports) presented at its input only the grains that the MESS egress port will transmit. By having all the data grain of a single timeslot presented to each MESS egress port and by providing the data grain selector with the ability to select up to N grains in single timeslot, the memory size can be reduced by a factor of N (see paragraph [0029] lines 5-10). Whereas Williams is not concerned with reducing the memory size or the hardware in general. Instead, Williams admits that the implementation of its design comes at a trade off between either speed or potentially significant additional hardware (see col.17 lines 45-55).

Moreover, amended claim 1 recites that selecting data grains is performed based on the ingress port associated with the received data grains and the position of the data in a group. This feature is also unique to the present invention because the selecting process in Williams is based on whether the receiving node is the destination node or not (see col.17 lines 13-22), and the samples are organized in a manner that avoids collision at the outputs not based on the ingress port associated with the received grains and their order in the group.

Accordingly, amended claim 1 is believed to be novel and inventive over Williams at least in view of the five features discussed above which are not disclosed or suggested by Williams. Withdrawal of the rejection under 35 USC 102 (e) is respectfully requested.

While claim 8 inherits all the features of claim 1 in view of its indirect dependency thereon, Applicants respectfully submit that the feature recited in claim 8 is novel in itself and patentable over Williams. Williams does not need to compact data as the buffers are arranged in series and only one data sample is read out and/or written in the buffer in a single timeslot. By contrast, the ingress processor of the present invention receives N grains at a time (being the aggregate of data grains) and selects up to N of them in a single timeslot to be written in the RAMs in parallel. A data compactor is used to ensure that there are no holes left in the RAM in the case where only a subset of the N grains is selected to be stored (see paragraph [0040]). As previously discussed in connection with claim 1, Williams does not disclose selecting a number of grains that equals the number of ingress ports. Thus, it is not possible that Williams discloses parallel storing of a variable number of data in different timeslots in a manner that leaves gaps in the RAMs. Accordingly, Williams fails to disclose the subject

matter of claim 8, and Applicants respectfully request withdrawal of the Examiner's rejection of this claim under 35 USC 102 (e).

Independent claims 13 and 16 have been amended similar to claim 1, and Applicants re-iterate the above arguments in support of their patentability.

With regard to the rejection of claims 14 and 15 under 35 USC 102 (e) in view of Williams, Applicants submit that the multiplexer of Williams is connected in a different way and does not provide the advantages achieved in the present application. The multiplexers, as recited in claims 14 and 15, are included in the egress processor in order to reduce the hardware size and number of ports (see paragraphs [0042] and [0053]) not at the inputs ports to output the samples of data one at each timeslot as in Williams (Figs.1 and 5). Withdrawal of the Examiner's rejection of these claims under 35 USC 102 (e) is respectfully requested.

Claims 4, 7, 10-12, and 18-20 are believed to be allowable and in compliance with 35 USC 102 (e) in view of direct or indirect dependencies on independent claims 1 and 16.

Claims 5, 6 and 9 are rejected under 35 USC 103(a) as being unpatentable over Williams in view of Bianchini (U.S. 7,031,330) on the basis of obviousness.

Claims 5 and 9 inherit all the features of independent claim 1 in view of their indirect dependencies from this claim. Independent claim 6 has been amended similar to claim 1. As discussed above, Williams fails to disclose the novel features of claim 1. Bianchini also is not concerned with reducing hardware and memory size. Bianchini fails to disclose aggregating all the data grains received at the ingress ports, and fails to provide the aggregate of data grains to the MESS egress ports simultaneously as recited in claims 1 and 6. Furthermore, Bianchini fails to disclose selecting, in one timeslot, a number data grains that equals the number of ingress ports, and that each MESS egress port selects only the data grains that it will transmit as recited in claims 1 and 6. Moreover, Bianchini fails to disclose selecting data grains in accordance with the ingress port associated with each grain and the position of each grain in its grain group.

Accordingly, each of independent claims 1 and 6 has been amended to include at least five features, which are not disclosed in any of the references cited in the Official Action. As none of these five features is taught or suggested, clearly the combination of all five features as in independent claims 1, and 6 cannot be taught or suggested by the cited references taken either alone or in combination. Applicants respectfully submit each of the independent claims now being submitted is believed to comply with 35 USC 103(a).

It is respectfully submitted that the Examiner has not provided a proper rejection of the above claims based on the rationale that there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art teachings to arrive at the claimed invention. It is respectfully submitted that the Examiner has not articulated the following:

1. a finding that there was some teaching, suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
2. a finding that there was reasonable expectation of success; and
3. whatever additional findings based on the Graham factual inquiries may be necessary, in view of the fact that the case under consideration, to explain the conclusion of obviousness.

It is respectfully submitted that the Examiner has not made all of these findings, and therefore this rationale cannot be used to support a conclusion that the claims would have been obvious to one of ordinary skill in the art.

As such, it is respectfully submitted that the claims as amended comply with 35 USC 103(a) and withdrawal of the rejections of the claims on that basis is respectfully requested.

Claims 5 and 9 are believed to be allowable in view of their direct or indirect dependencies on claims 1, 6.

Applicants respectfully submit that the amendments effected to the independent claims overcome each of the references cited in the Official action whether the references are taken alone or in combination.

Paragraph [0005] has been amended to better distinguish between ingress grains groups 100 and egress grain groups 106. Applicants respectfully request entry of this amendment which is not believed to introduce any new matter over that taught in the application as originally filed, as the amended paragraph relates to the prior art and not to the present invention.

It is respectfully submitted that the present application is now in condition for allowance and the Applicant looks forward to receiving an indication of patentability.

No fee is believed due for this submission. However, Applicant authorizes the Commissioner to debit any required fee from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP. The Commissioner is further authorized to debit any additional amount required, and to credit any overpayment to the above-noted deposit account.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

PLANTE, Patrice et al

By: /Curtis B. Behmann/

Curtis B. Behmann

Reg. No. 52,523

Borden Ladner Gervais LLP

World Exchange Plaza

100 Queen Street, Suite 1100

Ottawa, ON K1P 1J9

CANADA

Tel: (613) 237-5160

Fax: (613) 787-3558

E-mail: ipinfo@blgcanada.com

CBB/IT/cf